Abstracts

1/4 W Optical Receiver and Clock Recovery Circuit for Gb/s Digital Fiberoptic Links

A.S. Daryoush, X. Zhang and J.Y. Lin. "1/4 W Optical Receiver and Clock Recovery Circuit for Gb/s Digital Fiberoptic Links." 1996 MTT-S International Microwave Symposium Digest 96.2 (1996 Vol. II [MWSYM]): 891-894.

Design and simulation of a low power consuming MMIC chip set is presented in this paper., which is used as an optical receiver and clock recovery circuit operating up to 1.25Gb/s. This design is based on BTA24 Si BJT transistor array from Bipolarics. Major design innovations such as push-pull self-oscillating mixer and a push-push frequency doubler is used to provide a total power consumption of 247mW in an area of only 700µmx700µm.

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